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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,965	06/20/2001	Hirofumi Honda	05721.0025	4448

22852 7590 05/07/2003

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EXAMINER

AMINI, JAVID A

ART UNIT	PAPER NUMBER
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2672

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DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary

Application No.

09/883,965

Applicant(s)

HONDA ET AL.

Examiner

Javid A Amini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 1-3 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: _____

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, and further in view of Kawabata (us 6,373,533 B1).

1. Claim 1.

“A luminance level compensating apparatus comprising: a first masking device for passing only a luminance signal corresponding to a pixel in a first detection range in the vertical direction of an image which is indicated by an input luminance signal; a second masking device for passing only a luminance signal corresponding to a pixel in a second detection range including said first detection range in the vertical direction of the image which is indicated by said input luminance signal; a first histogram memory device for detecting and storing a first frequency for each luminance level of the luminance signal output from said first masking device for each predetermined period; a second histogram memory device for detecting and storing a second frequency for each luminance level of the luminance signal output from said second masking device for each predetermined period; a frequency data mixing device for generating mixed frequency data based on each of the first and second frequencies of said first and second histogram memory devices; and a compensating device for compensating the luminance level of said input luminance signal based on said mixed frequency data”,

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Tanaka teaches in (col. 4, lines 27-33) and see Figs. 4, 6, a masking signal generator circuit 17 generates two masking signals M_1 , M_2 for masking a part of the screen on the basis of the vertical blanking pulse V-P supplied thereto, and applies them through two masking signal supply switches 28, 29 to the luminance signal amplifier circuit 12 and the peak detector circuit 14. The first and second masking devices covered by (circuit 17 in Fig. 4, that is SN74ALS123 commercial advanced low-power Schottky logic. These elements equipped with different types of gates that have two inputs and one output, the two inputs multiply the data frequency in AND gate and add the two inputs in OR gate and they are equipped with small memory area). The step of luminance signal corresponding to a pixel in first and second detection is obvious because the video circuit controlling the brightness (luminance) of the pixel. But Tanaka does not explicitly specify the histogram generator (histogram memory device), however, Kawabata teaches in (col. 1, lines 35-49) in the circuit shown in Fig. 6, the histogram generator 1 creates, for example, a histogram with four intervals. In this case, if an image of a person standing against a dark background as shown in Fig. 8 is the input, then the histogram output from the histogram generator 1 represents frequencies H_1 , H_2 , H_3 , and H_4 corresponding to intervals S_1 , S_2 , S_3 , and S_4 as shown in Fig. 7. In Fig. 7, the input video signal level S is plotted along the abscissa and the frequency F is plotted along the ordinate. Kawabata illustrates in Figs. 3-4, two histograms (L_2 and L_3) for detecting and storing frequencies (H_1' - H_4' and H_1'' - H_4'') for each luminance level of the luminance signal output.

The generating mixed frequency data, Kawabata teaches in (col. 3, lines 33-67) a certain value is added to the frequency H_3 of the interval S_3 containing the picture level for displaying the face in the histogram, and then an adjustment value c is subtracted from the frequency of the other

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intervals. The video signal correction circuit 4 uses this corrected histogram for correcting the input video signals. Accordingly, the frequency H3 of the area S3 containing the picture level for displaying the face is intensified to improve the contrast of this portion.

The compensating (correcting) the luminance level, Kawabata teaches in (col. 2, lines 20-28), a tone correction (compensating) circuit corrects the tone of video signals by using a histogram. A controller in turn corrects the histogram again, which is adjustable. The controller is adjusted as required for intensifying the input/output video signal characteristic of the picture level in certain areas of importance to the user. Thus, the tone of video signals is corrected using corrected histograms.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kawabata into Tanaka in order to combine circuit configuration of Fig. 2 of Kawabata to circuit configuration of Fig. 3 of Tanaka, to provide for adjusting histograms and masking signals.

2. Claim 2.

“A luminance level compensating apparatus according to claim 1, wherein each of said first and second histogram memory devices detects and stores said first and second frequencies for each field period, and said frequency data mixing device generates said mixed frequency data for each field period”, the step of histogram memory devices is obvious because Tanaka illustrates comparison between two masking signals in different levels in Fig. 6, it means in order to be able to compare, a device should be equipped with storage area. And also Tanaka teaches in abstract that a histogram correction circuit calculates a look-up table, and a video signal correction circuit corrects the tone of the video signals using the look-up table (the LUT is stored somewhere). On

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the other hand Kawabata illustrates in Figs. 3-4 different histograms with different frequencies for each intervals.

3. Claim 3.

“A luminance level compensating apparatus according to claim 1, wherein said frequency data mixing device includes a multiplying device for multiplying the frequency for each luminance level stored in said first histogram memory device by a coefficient; and a selecting device for comparing the frequency for each luminance level output from said multiplying device with the frequency stored in said second histogram memory device for each luminance level and for outputting a smaller frequency of the compared frequencies as the frequency data for each luminance level of said mixed frequency data”, the step is obvious because Tanaka illustrates in Fig. 4 item 17 that is (SN74ALS123) commercial advanced low-power Schottky logic. These elements equipped with different types of gates that have two inputs and one output, the two inputs multiply the data frequency in AND gate and add the two inputs in OR gate and they are equipped with small memory area.

Conclusion

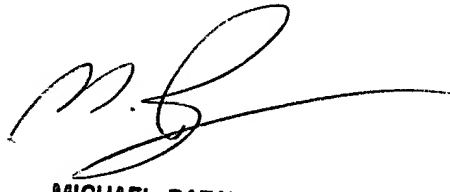
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-8705 for regular communications and 703-746-8705 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Javid A Amini
Examiner
Art Unit 2672

Javid Amini
April 29, 2003


MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
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